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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/801,501	03/12/2004	Dong-Han Kim	9903-075	1864
20575	7590	09/06/2006	EXAMINER	
MARGER JOHNSON & MCCOLLOM, P.C. 210 SW MORRISON STREET, SUITE 400 PORTLAND, OR 97204			DIAZ, JOSE R	
			ART UNIT	PAPER NUMBER
			2815	

DATE MAILED: 09/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/801,501

Applicant(s)

KIM, DONG-HAN

Examiner

José R. Díaz

Art Unit

2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 22 June 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,4-7,10,11,14-17,19 and 20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,4-7,10-11,14-17,19 and 20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on June 22, 2006 has been entered.

Claim Objections

2. Claim 1 is objected to because of the following informalities:
- Please delete the term "being" between "...a plurality of test pads electrically" and "connected to..." in line 7 of claim 1.
 - Please delete the phrase "the respective chip pads, the respective test pads," between "...for testing electrical properties of the integrated circuits," and "the respective chip pads and test pads being..." in line 8 of claim 1.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

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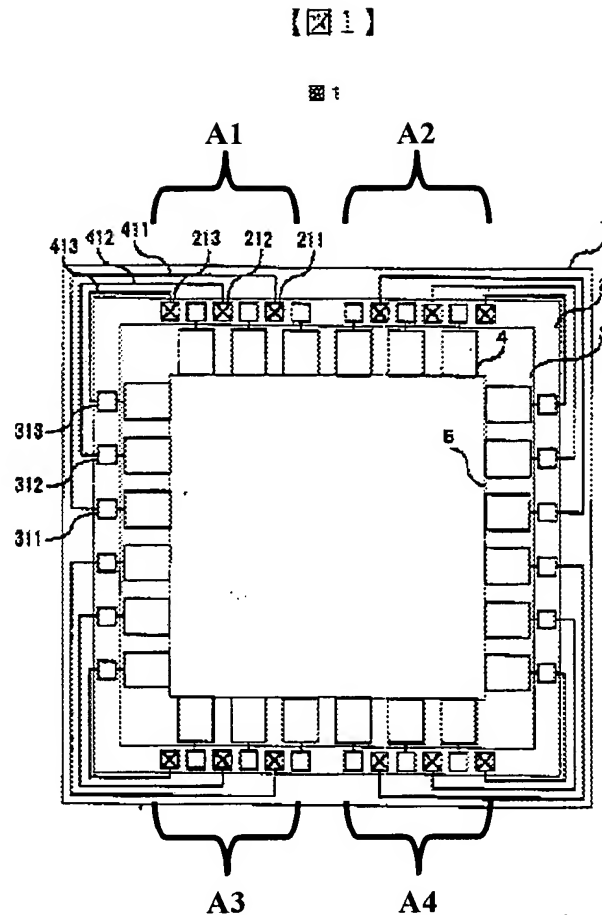
(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 4-7, 10-11, 14-17 and 19-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Aiki et al. (JP 2002-303653).

Regarding claims 1 and 11, Aiki et al. teaches a semiconductor chip comprising:
a plurality of outer edges (consider the corners of chip 1, as shown in fig. 1);
a peripheral area (2) located adjacent to the outer edges [see fig. 1]; and
a main circuit area (5) located within the confines of the peripheral area, the main circuit area including integrated circuits [see fig. 1],

wherein the peripheral area includes chip pads (squares without X marks such as 311-313) connected to the integrated circuits [see fig. 1], a plurality of test pads (the X marked squares such as 211-213) electrically connected to the integrated circuits for testing electrical properties of the integrated circuits [see fig. 1], the respective chip pads and test pads being arranged in four rows (consider rows A1, A2, A3 and A4) at substantially uniform intervals [consider adjacent X-marked and Non-marked squares in each row A1, A2, A3 and A4, which are spaced at "substantially uniform intervals." See fig. 1], the chip pads being arranged in each of the rows adjacent the main circuit area of the semiconductor chip [see fig. 1], and the test pads being located within each of the rows of chip pads [see fig. 1], and the test pads are substantially the same dimensional size as the chip pads [see fig. 1].

In addition and with regards to claim 11, Aiki et al. teaches a tape wiring substrate (1) [see fig. 1].



Regarding claims 4 and 14, Aiki et al. further teaches that the test pads are located at the ends of the rows of chip pads [consider the X marked squares in each row A1, A2, A3 and A4, such as 213 in figure 1].

Regarding claims 5 and 15, Aiki et al. further teaches that the configuration of the main circuit area (5) is arranged to form corners (consider the corners of area 5), and the test pads are located near the corners of the main circuit area [consider the X marked squares in each row A1, A2, A3 and A4, such as 213 in figure 1].

Regarding claims 6 and 16, Aiki et al. further teaches that the chip pads (squares without X marks within rows A1, A2, A3 and A4) are arranged in rows parallel to at least one set of opposed outer edges of the semiconductor chip, and the test pads (the X marked squares within rows A1, A2, A3 and A4) are arranged within the rows of chip pads [see fig. 1].

Regarding claims 7 and 17, Aiki et al. further teaches that the test pads (the X marked squares within rows A1, A2, A3 and A4) are arranged between the rows of chip pads (the squares without X marks in rows A1, A2, A3 and A4) [see fig. 1].

Regarding claim 10, Aiki et al. further teaches that the chip comprises one of an edge-pad-type chip and a center-pad-type chip (5) [see fig. 1].

Regarding claims 19-20, Aiki et al. further teaches that the tape wiring substrate comprises an insulating base film (1300), wiring patterns (1400) formed on the insulating base film, leads (1511) formed integrally with the wiring patterns, and dummy leads (1520) electrically isolated from the wiring patterns [see fig. 21 (b)].

Response to Arguments

5. Applicant's arguments with respect to claims 1, 4-7, 10-11, 14-17 and 19-20 have been considered but are moot in view of the new ground of rejection.

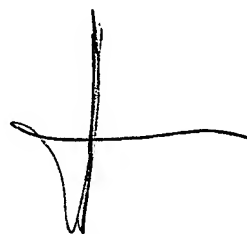
Correspondence

Any inquiry concerning this communication or earlier communications from the examiner should be directed to José R. Díaz whose telephone number is (571) 272-1727. The examiner can normally be reached on Monday through Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Parker can be reached on (571) 272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

José R. Díaz
Examiner
Art Unit 2815

A handwritten signature in black ink, appearing to be 'K Parker', with a stylized vertical line and a horizontal crossbar.

KENNETH PARKER
SUPERVISORY PATENT EXAMINER